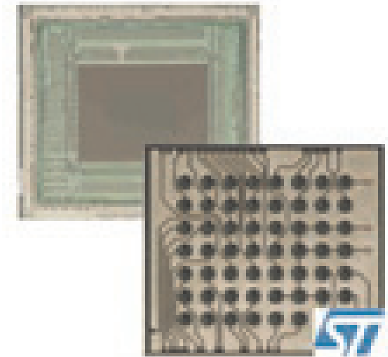
3D-IC & TSV Interconnects

2010 Reports

> One report update making the business case for 3D IC Packaging
> One new report to understand 3D TSV via process options

MARKET TRENDS

The continuation of Moore's law by conventional CMOS scaling is becoming more and more challenging, requiring huge capital investments. 3D Packaging with 3D TSV interconnects provides another path towards the "More than Moore", with relatively smaller capital investments. Despite the impact of the economic downturn, 3D integration investments are strategic innovations and have continued.

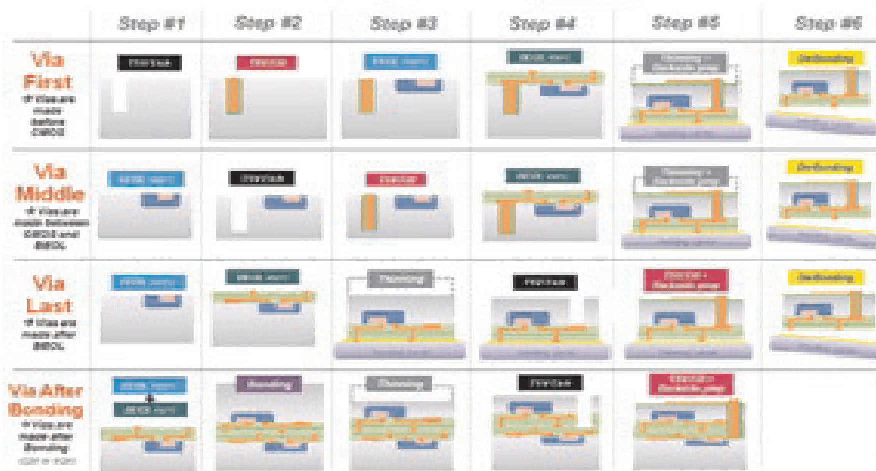


STMicroelectronics CMOS image sensor WLP with 3D TSVs

We have identified as of today **more than 15 different 300mm 3-D IC pilot lines** running or currently being installed world-wide (within R&D centers, at packaging houses, CMOS foundries or within IDM fabs). This year, several initiatives of key industry leaders happened such as STMicro for 3D integration in MEMS and CMOS image sensors, Elpida for stacked DRAM memories and Sony with the introduction of Backside illuminated (BSI) technology into its camera sensor products portfolio.

Strong dynamics in MEMS, CMOS image sensors, memory, analog and logic industries continue and will drive adoption of 3D TSVs to high volumes within the next decade. Additionally, **new applications such as HB-LED silicon modules, Solar and Power components** are also on the point to catch the 3D TSV trend and to benefit from this disruptive interconnect technology!

BUT CHALLENGES ARE STILL AHEAD!



Courtesy of Yole Developpement

3D infrastructure & supply chain is the biggest immediate issue we have identified for the broad adoption of 3D ICs. As many scenarios are possible for the implementation of 3D TSV interconnects (via first / via middle / via last / via after bonding), a big question at the moment is WHO will take the risk to invest and will have the ownership of the realization of the different 3D TSV process steps (to be implemented in front-end, mid-end, back-end…)? As a result, we have decided to release this year one new report called "3D TSV Technologies & Scenarios: Via First or Via Last?". The analysis is focusing on the deeper understanding of the rationale behind these strategic technology choices to be made. It puts into perspective who is doing what at the moment, what alliances are forming at the horizon, which technology choices have already been made and for which applications?

I/O standardization between interfaces such as memory to digital layers is also a serious issue that needs to be fixed rapidly. Indeed, 3D integration of memory + logic ICs together is perceived as the next big wave for volume adoption of 3D TSV in the near future. Multiple applications are targeted, including CPU, GPU, DSP, FPGA, ASICS and Basebands ICs that will be used in future cell phones, super-computers, network / storage systems, notebooks, automotive and medical processing units among others. **Thermal management and reliability** could also reduce 3D ICs application space in the longer run. However, different solutions are currently underway in response to this possible challenge.

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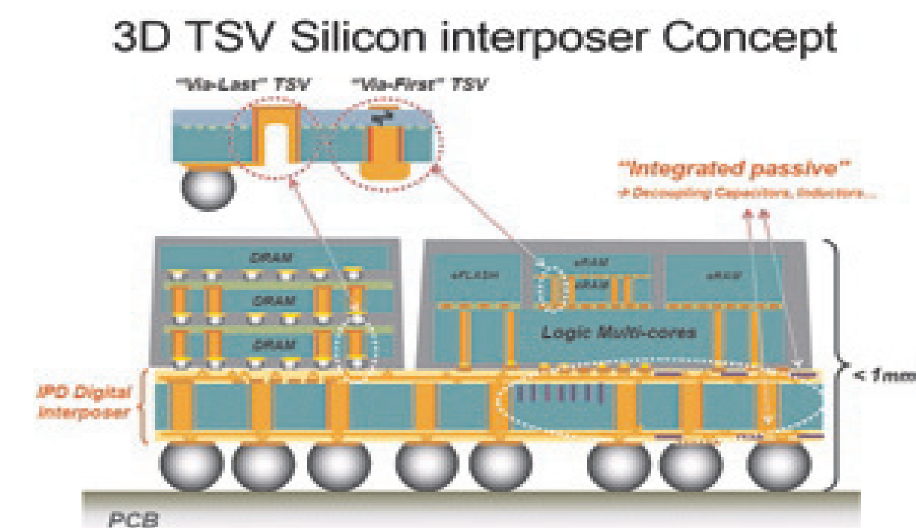
MORE SILICON VALUE IS MOVING TO THE PACKAGE

A recent trend more and more these days are **3D interposers**. Based on silicon or glass, 3D interposers are next generation substrate technology which aims at replacing traditional PCB laminate or ceramic technologies for the sake of extreme miniaturization and performance. This type of "intermediate 3D" is perceived as a "bridge" platform between today's 2D and future genuine 3D that will start beyond 2012-2013. Specific features like the integration of mature logic and analog functions such as IPD (integrated passive devices) will be key components in the effective commercialization of 3D interposers in the short term.



3D integration opens up a possible **supply chain value change** to all players as more and more value is now moving to the package in general. IDMs, Fab-less players, wafer foundries, packaging houses, MEMS players, substrate and PCB suppliers are all poised to take on more value in this new era if they all prepare for the investments it requires.
It is also astonishing to notice the **rapid evolution of 3D thinking** within the IC community: two years ago, the big unceasing question was "Why 3D?". Today, moving forward with the concrete implementation of the technology, questions are now "When 3D?" and "How 3D?". It is terrific to realize that in less than one decade from now, looking back at what has happened, we will be wondering "Why 2D?"

KEY FEATURES OF THE REPORTS

- **Revamped market forecasts & technology roadmaps for 3D IC components:**
  - Impact of the economic downturn on the 3D TSV market
  - Market forecast update for MEMS, CMOS image sensors, logic, analog and memory applications
  - New application areas covered: HB-LED modules, power and solar components
  - Business case for 3D interposers: applications, market and players
- **3D IC players 2008 market shares & revenues breakdown in $M (as packaging services or estimated in relative packaging value)**
- **Supply chain perspectives, key players and emerging infrastructure for 3D Packaging**
- **Strategic technology choices for 3D integration scenarios:**
  - Analysis of the different possibility for the implementation of TSVs and the rationale behind (via first / via middle / via last / via after bonding)
  - Analysis of the cost structure for different implementation cases (vias in front-end, vias at packaging assembly house, C2W versus W2W, …)

WHO SHOULD BUY THIS REPORTS ?

- **Integrated semiconductor Device Manufacturers and fabless semiconductor companies**
  - Benchmark the status of 3D integration within the industry
  - Identify possible partnership for your forthcoming developments and find second source packaging subcontractors for your 3D TSV components
- **Assembly and Test Service companies**
  - Get the list of the main 3D IC players and users
  - Screen possible new 3D integration applications to support diversification strategy
- **Equipment and Material suppliers**
  - Understand the differentiated value of your products and technologies in this market
  - Identify new business opportunities and prospects
- **Electronic module makers and Original Equipment Manufacturers**
  - Evaluate the availability and benefits of using 3D components in your end system
  - Monitor different 3D component suppliers to adjust your sourcing strategy
- **PCB / IC substrate manufacturers**
  - Monitor the evolution of IC Packaging & Assembly, especially linked to the emerging 3D TSV interposers, IPD and chip embedding PCB-based technologies
- **IC and MEMS Foundries**
  - Spot new opportunities & define diversification strategies by reusing your infrastructure and expertise within the 3D Packaging market

3D IC & TSV INTERCONNECTS:
Business update - 2010 report

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3D TSV TECHNOLOGIES & SCENARIOS:
Via first or Via last? - 2010 report

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BIO

Jérôme Baron is leading the MEMS and Advanced Packaging market research at Yole Développement. He has been involved in the technology analysis of the 3D packaging market evolution at device, equipment and material levels. He was granted a Master of Science degree in Micro & Nanotechnologies from the National Institute of Applied Sciences in Lyon, France.

BIO

Jean-Marc Yannou recently joined Yole Développement as technology and market expert in the fields of Advanced Packaging and Integrated Passive Devices. He has 15-years of experience in the semiconductor industry. He worked for Texas Instruments and Philips (then NXP semiconductors) where he served as Innovation Manager for System-in-Package technologies.

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- Photovoltaic
- Microfluidics
- 3D IC/TSV & Advanced Packaging

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