Fan-Out and Embedded Die: Technologies & Market Trends
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The main objectives of this report are the following:

- To update the business status of both embedded wafer level package technologies (FOWLP and Embedded Die Package) markets
- To provide a market forecast for the coming years, and estimate future trends
- To analyze key market drivers, benefits and challenges of embedded wafer level packages by application
- To describe the different existing technologies, their trends and the roadmaps

The FOWLP and Embedded Die Package markets are studied from the following angles

- State-of-the-art technology and trends
- End-user applications and drivers
- Market value
- Industrial supply chain & value chain
THE EVOLUTION OF SEMICONDUCTOR PACKAGING

A bridging technology between ICs and PCBs

Packaging fills the gap in between ICs and PCBs improvement speeds

- **1970**: Through hole technology
- **1980**: Surface mount devices
- **1990**: CSPs/BGAs, SiPs
- **2000**: WLCSP, more SiPs, Flip Chip BGA, PoP
- **2010**: 3DIC, TSV, Fan-out WLCSP, Cu pillars, Silicon interposers

Feature sizes: CMOS transistors 28nm

Feature sizes of PCBs

Development in CMOS processing capabilities

Development in PCB processing capabilities

PACKAGING ADDED VALUE:

More Moore and More than Moore

3D approach allows to get all the benefit from chip miniaturization and package integration.

3D integration is seen today as a new paradigm for the future of the semiconductor industry, as it will enable several more decades of chip evolution at ever lower cost, higher performance and smaller-size features.
Numerous market drivers lead to a WLP solution

WAFFER-LEVEL-PACKAGING MARKET DRIVERS

- **Cost**
  - Lower packaging cost
  - Lower test cost

- **Form-factor**
  - Smaller thickness
  - Lower footprint

- **I/Os density**
  - Lower pitches
  - No standard
  - Smaller dies
  - Higher density of I/Os

- **Integration**
  - IPD
  - SIP
  - 3D

- **Electrical performance**
  - Smaller Interconnect lines
  - Higher frequencies
  - Higher packaging speed
  - Lower parasitics

- **Thermal performance**
  - Lower power consumption
  - Higher package density

There are two main substrate types for embedding technologies:

- **FOWLP** is based on a reconfigured molded wafer infrastructure.
- **Embedded die in package** is based on a PCB type of panel infrastructure.

A different approach depending on substrate type:
FAN-OUT WLP PRINCIPLE

Embedding in a molding compound allows thin packaging.

- Tape lamination
- Pick and place
- Wafer level molding
- Carrier removal / de-bonding
- Standard WLB process (Passivation, pattern, RDL, bonding)
- Dicing
- Carrier with foil and chips
- Molding with liquid mold compound
- Reconstituted wafer after molding
- WLP Fan-Out wafer
- After singulation

Source: Infineon
Numerous advantages position FOWLP as a promising solution.

- Smaller footprint and thinner package than Flip-Chip BGA
- Lower thermal resistance compared to Flip-Chip BGA
- Fan-out zone adaptable to customer needs
- Reliable, miniaturized high performance package
- High degree of package design freedom
- Shorter interconnections
- No restriction in bump pitch
- No laminate substrate required
- Better board level reliability compared to WL-CSP
- RoHS and REACH compliant package
- Excellent electrical performance
- Simplified supply chain and manufacturing infrastructure
- Smaller footprint and thinner package than Flip-Chip BGA

A lot of products are already packaged using Fan-in solution which is cheaper than Fan-Out.

With die size reduction and higher pins count, manufacturers will have two options:

- Reducing ball pitch in order to have more connections within the die surface.
- Going Fan-Out and allowing an easier redistribution.

Since pitch reduction is very challenging, Fan-Out approach is offering a good opportunity.

FOWLP has a sweet spot area where Fan-In cannot fit.
FAN-OUT POTENTIAL APPLICATIONS

Opportunities for FOWLP in mobile phones

Orange: Devices that can be found in FOWLP packages today

Green: Devices that could be found in the future in FOWLP

Grey: Devices that will likely remain on WLCSP or flip-chip package or move to 3DIC

Discrete passives

FOWLP has the potential to fit in many applications

FOWLP ACTIVITIES: GLOBAL MAP OF MAIN PLAYERS

FOWLP catches the interest of many companies.
**FAN-OUT WLP: TECHNICAL CHALLENGES**

- **Topography**
  - Due to different sizes of devices, the shaping non-planarity can become an issue for WF integration.

- **Chip-to-mold non-planarity**
  - Die alignment at the interface can lead to BGA deformation.

- **Warpage**
  - The mismatch in forming pressure along the molding process step may cause issues with the packaging and the device can impact under bump metallurgy and strains on dies.

- **Reliability**
  - In case of design changes, thermal stress and alignment issues may cause device warpage and device failures.

- **Die shift**
  - Lack of alignment in the substrate during pick and place induces challenges for lithography steps and alignments.

**FOWLP technical challenges to overcome**
**TECHNOLOGY ROADMAP FOR FOWLP**

### Key parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
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<tbody>
<tr>
<td>Maximum package size</td>
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<tr>
<td>Max level of RDL</td>
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<tr>
<td>Line/Space</td>
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<tr>
<td>Package minimum thickness (with BGA)</td>
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<tr>
<td>Minimum die side size</td>
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<tr>
<td>Minimum mold clearance distance</td>
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<tr>
<td>Minimum bump pitch</td>
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<tr>
<td>Minimum die-to-die distance</td>
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Roadmap of FOWLP follows the high demanding expectations from the market.

A high growth is expected

FOWLP activity revenues (M$)
Overall evolution since eWL B technology introduction

- CAGR ~ 10%
- Transition phase
- Ramp-up with fab-less wireless IC players and wide FOWLP infrastructure/supply-chain

Yole Developpement ©

FO-WLP revenues (M $)

- CAGR > 30%
- Intel Mobile/Infineon eWL B-driven

$0M $300M $600M $900M


EMBEDDED DIE PACKAGING PROCESS FLOW

Example with “chip-first – face-up” approach

1) Die Bonding
   - Adhesive on copper foil

2) Lamination
   - Pick & place on copper foil
   - Relamination process

3) Laser drilling

3) Structuring
   - Copper plating, imaging and etching

Principle of embedded die package in substrate

Source: AT&S

Embedded Die package advantages

- Good for copy protection
- New suppliers
- Low manufacturing costs thanks to very mature products
- Reduced parasitics thanks to short interconnections
- High potential for reducing I/Os thanks to design (wire-bond layout)
- High potential for components integration
- Small footprint thanks to more space given to surface components
- High mechanical reliability
- Improved thermal performance thanks to proximity with active
- High design flexibility since chip can be positioned wherever we want
- Reduced parasitics thanks to short interconnections

Embedded Die Packaging

Technical challenges

- Warpage
- Resolution
- Yield
- Die positioning
PCB manufacturers can create a new supply chain in semiconductor industry

1) Die Customization (IDM or Wafer Level Technology Provider)
   - Embedded Die Customization
   - Wafer thinning
   - Wafer sort / Die preparation

2) Embedded Die Substrate Fabrication (PCB manufacturer)
   - Embedded Die PCB sort
   - Component placement
   - Multi-layer build up fabrication
   - PCB Core Fabrication

3) Product level assembly and final testing
   - Solder paste print
   - Component placement and reflow
   - Product level assembly and test

- Supply chain and responsibilities can be defined case by case upon players will of implication
- Embedded die packaging opens the door for substrate suppliers to realize the whole packaging, assembly and test themselves → Good opportunity for substrate suppliers to create new business and potential threat for OSATs market
Today, Embedded Die Packaging technology only targets low-cost, low I/O pin-count applications (mainly power and analog ICs).

However, to enter the digital space and more complex SiP module realization, embedded die technologies are set to evolve.

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<tr>
<td>Pad Pitch on die</td>
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<tr>
<td>Chip layer stacking</td>
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<td>Line/Space</td>
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<tr>
<td>Package minimum thickness</td>
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</tr>
<tr>
<td>Chip thickness (min-max)</td>
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Embedded die package market is still a niche. The revenues forecast (M$) for embedded die packages shows a steady increase over the years from 2010 to 2020, reaching $300M in 2020. The overall evolution since technology introduction is marked by a consistent growth trend.
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