Press Release
July 20th, 2021
LYON, France

System-in-Package industry: IDMs, OSATs, and foundries are taking the advantage[1]

Through enabling design and supply chain agility, SiP will reach more than $19B by 2026.

OUTLINE:

- Market forecasts:
  FC[2] & WB[3] based SiP[4] market is expected to reach to US$17 billion in 2026 with 5% CAGR[5]$_{20\text{-}26}$.
  ED[6] SiP is expected to reach $189M in 2026, at a 25% CAGR $_{20\text{-}26}$.
  FO[7] SiP market value is expected to reach US$1.6 billion in 2026 at a rate of 6% CAGR$_{20\text{-}26}$.
- Technology trends:
  The FO platform is viewed as one of the top packaging options for SiP.
  Flip-chip and IC[8] substrates: the industry needs strong motivation to develop new substrate processing technology in order to scale further.
  ED technology is still in its early years in terms of adoption.
- Supply chain:
  SiP's ecosystem has matured in last five years with majority of share consolidated to the top OSATs such as ASE, Amkor, and JCET in RF[9] space.
  This consolidation will remain for future years.
  Amkor, ASE, and JCET are projecting estimated 10-20%+ increase in revenue from SiP business in 2021 compare to 2020.

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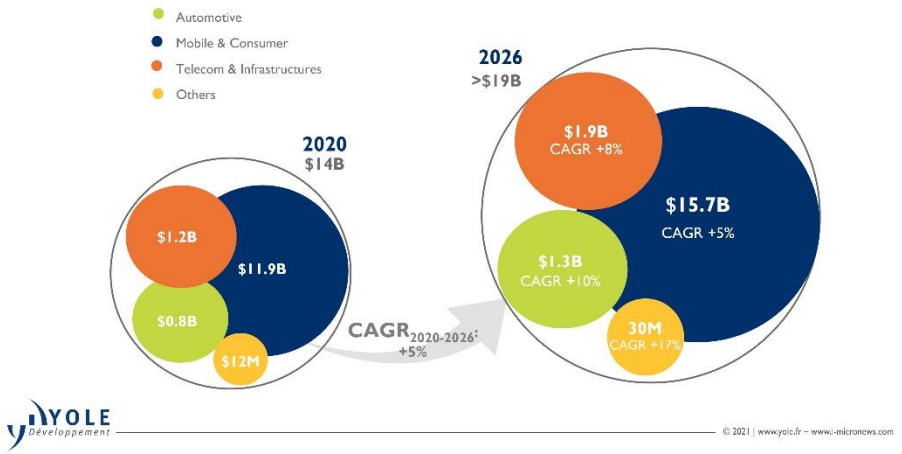
[1] Extracted from:
System-in-Package Technology and Market Trends 2021 report, Yole Développement
Smartphone Design Win Quarterly Monitor, System Plus Consulting, Q1 2021
[2] FC: Flip Chip
[3] WB: Wire-Bond
[4] SiP: System-in-Package
[5] CAGR: Compound Annual Growth Rate
[6] ED: Embedded Die
[7] FO: Fan-Out
[8] IC: Integrated Circuit
[9] RF: Radio Frequency

"SiP has become synonymous with technologies ranging from high-end die-to-die chiplet-type advanced integration to devices found in mobile handsets with increased integration and functionality leveraging best-in-class advanced packaging processes." asserts **Vaibhav Trivedi, Senior Technology & Market analyst, Packaging, within the Semiconductor, Memory & Computing division at Yole Développement (Yole).** He adds: *"The SiP platform is crucial in achieving 'More than Moore' in the race for heterogeneous integration, where advanced packaging remains at the forefront with front-end technology."*

The SiP market is expected to increase from US$14 billion in 2020 to US$19 billion+ in 2026. The SiP product line includes high- to mid-end SiP devices, such as computing and data center applications, with much higher margins than the low-end SiP devices found in mobile handsets. High-end SiP market segment is expected to grow at a 9% CAGR between 2020 and 2026, whereas the low-end RF SiP one, found in mobile phones, is expected to grow at a slightly lower CAGR of 5% from 2020 to 2026.

2020-2026 System-in-Package market forecasts
Breakdown by market segment

(Source: System-in-Package Technology and Market Trends 2021 report, Yole Développement, 2021)



In this dynamic context, Yole and System Plus Consulting, both part of Yole Group of Companies, investigate disruptive semiconductor technologies and related markets in depth. They point out the latest innovations in the packaging industry and underline the business opportunities.

Released today, the System-in-Package Technology and Market Trends 2021 report from Yole describes technologies that can be classified as "System-in-Package", identifies and details the SiP platform's key process steps. Including market trends and forecasts, supply chain, technology trends, technical insights and analysis, take away and outlook, this study also delivers an in-depth understanding of the ecosystem and main players' strategies.

In addition, the Smartphone Design Win Quarterly Monitor from the reverse engineering and costing company, System Plus Consulting, utilizes data from representative phones (65+

phones per year torn down in the System Plus Consulting Phone Teardown Track Module) and follows the OEM market share. The monitor provides the detailed design wins and related supply chain for the eight phones being analyzed, along with supply chain alternatives for the main devices. It also delivers added value analysis of the packaging technologies selected by the leading smartphone manufacturers and their suppliers.
Yole and System Plus Consulting present today their vision of the SiP technologies and related markets.

In the new System-in-Package Technology and Market Trends 2021 report, SiP solutions are differentiated into three categories:

- The dominant flip chip/wire bond-based packaging form factors
- FO based multi-die form factors
- And the ED form factors.

The SiP remains a crucial platform as it allows the OEM[10] customer to integrate one or more functionalities onto a substrate-based package instead of integrating it as a discreet component on the PCB[11]. The compact and miniaturized package is ideal for mobile handset devices. SiP provides flexibility and freedom to the designers in terms of sourcing the die and passive components for best-in-class cost and performance benefits. With the rise in SiP devices, many device wafers have adopted flip chip bumping or ball drop processes as these can be easily attached in SiP Packages, instead of using a wire bonding process to attach a die. WLCSP[12] components have risen mainly due to the SiP platform's capability to integrate such varied form factors in a single package.
According to **Favier Shoo, Team Lead Analyst, Packaging, within Semiconductor, Memory and Computing Division at Yole**: *"In terms of technology and a roadmap, the SiP platform continues to push the boundary in the race to produce denser, thinner, and smaller form factors. These new process technologies include double-side molding technologies that eliminate the underfill operation from the bottom die resulting in an improved cost structure and manufacturing efficiencies".*
In addition to dual side molding, compartmental and conformal shielding remains another key process technology for RF-SiP devices. In terms of package height, OSATs are expected to push for 0.6 mm total package height for SiP devices in the coming years. With the deployment of 5G, increased development of materials is seen, to improve the reliability of SiP devices, especially in molding and solder ball materials.
Favier Shoo adds: *"We can expect the industry to push the boundary of chip shooter tools to enhance the accuracy of component placing and throughput. In addition, we can also expect novel,*

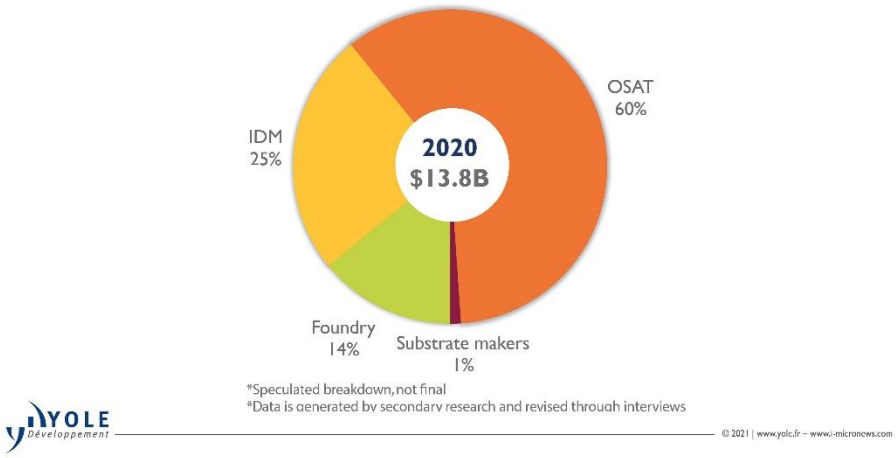
[10] OEM: Original Equipment Manufacturer
[11] PCB: Printed Circuit Board
[12] WLCSP: Wafer Level Chip Scale Package

reliable packaging materials to set the stage for the next set of SiP devices to drive heterogeneous integration further".

SiP global business models have evolved significantly over the past five years. OSATs have dominated in the past, and the demand was somewhat scattered in the SiP landscape 5-8 years ago. However, with mobile handsets, RF evolution, and 5G deployment, SiP has come of age and can robustly support multiple markets, starting with the low-end RF SiP markets dominated by top OSATs and driven by leading OEMs, such as Apple and Samsung.

2020 total SiP market share: packaging revenue, business model*

(Source: System-in-Package Technology and Market Trends 2021 report, Yole Développement, 2021)



In this regard, Yole's partner, System Plus Consulting, made a special focus dedicated to the RF technologies and SiP solutions in its Smartphone Design Win Quarterly Monitor Q1 2021. System Plus Consulting's analysis offers a clear view of the market leading semiconductor companies and a direct comparison between OEMs.

The high-end SiPs remain on a higher growth trajectory with post-pandemic demand accelerating infrastructure spend globally. This explosion in multiple segments has prompted IDMs, foundries, EMS houses, and OSATs to compete in this thriving market.

ASE's USI generates a significant portion of ASE's revenue and will approach 50% of the revenue in a few years.

OSATs are developing capabilities to mount anywhere from 50-100 passive SMT components and manage a supply chain that was foreign to them just a few years ago.

IDMs, such as Intel and Samsung, are driving hybrid die-to-die interconnect-stacked-packaging, such as Intel's Foveros architecture and Samsung's x-cube architecture. These die-to-wafer or die-to-die interconnects will gravitate towards hybrid bonding, improving device performance and bandwidth in a near future. Intel is also targeting a Co-EMIB server product on 7 nm node by 2023.

These advances in the high-end SiPs are here to stay, and increased M&A is expected within the top IDMs and foundries to increase their capabilities to develop these product lines in the best cost/performance envelope.

All year long, Yole Group of Companies, including System Plus Consulting and Yole Développement publishes numerous advanced packaging reports and monitors. In addition, experts realize various key presentations and organize key conferences.

In this regard, discover the 3D Packaging is transforming the world of Semiconductor Packaging – Webcast replay on i-Micronews.
Make sure to be aware of the latest news coming from the industry and get an overview of our activities, including interviews with leading companies and more on i-Micronews. Stay tuned!

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About our analysts

Vaibhav Trivedi is a Senior Technology & Market analyst at Yole Développement (Yole) working with the Semiconductor, Memory & Computing division. Based in the US, he is a member of Yole's advanced packaging team and contributes to analysis of ever-changing advanced packaging technologies. Vaibhav has 17+ years of field experience in semiconductor processing and semiconductor supply chain, specifically on memory and thermal component sourcing and advanced packaging such as SiP and WLP. Vaibhav has held multiple technical and commercial lead roles at various semiconductor corporations prior to joining Yole. Vaibhav holds a Bachelor of Science in Chemical Engineering, and Master of Science of Material Science from University of Florida in addition to an MBA from Arizona State University.

Favier Shoo is a Team Lead Analyst in the Packaging team within Semiconductor, Memory and Computing Division at Yole Développement (Yole), part of Yole Group of Companies. Based in Singapore, Favier manages an international team and develops the technical expertise and market know-how within the team. Favier also focuses on the production of technology & market reports, conducts strategic consulting and custom studies. As an acknowledged professional in the semiconductor packaging market space, Favier is regularly engaged in international conferences, with presentations, keynotes, and panel review sessions. During 7 years at Applied Materials as a Customer Application Technologist in the advanced packaging field, Favier developed an in-depth understanding of the supply chain and core business values. Prior to that, Favier worked at REC Solar as a Manufacturing Engineer to maximize production. Favier holds a Bachelor's in Materials Engineering (Hons) and a Minor in Entrepreneurship from Nanyang Technological University (NTU) (Singapore). Favier was also the co-founder of a startup company where he formulated business goals, revenue models and marketing plans.

Romain Fraux is the CEO of System Plus Consulting of Yole Développement. System Plus Consulting focuses on Reverse Costing analysis of electronics, from semiconductor devices to electronic systems. Supporting industrial companies in their development, Romain and his team are offering a complete range of services, costing tools and reports. They deliver in-depth production cost studies and estimate objective selling price of a product, all based on a detailed physical analysis of each component in System Plus Consulting laboratory. Romain has been working for System Plus Consulting for more than 15 years and was previously the company's CTO.He holds a bachelor's degree in Electrical Engineering from Heriot-Watt University of Edinburgh (Scotland), a master's degree in Microelectronics from the University of Nantes (France), and a Master of Business Administration.

About the report and monitor

System-in-Package Technology and Market Trends 2021

Through enabling design and supply chain agility, System-in-Package (SiP) will reach $19B by 2026, with IDMs, OSATs, and foundries taking advantage of it. – Performed by Yole Développement

Smartphone Design Win Quarterly Monitor

The first-ever smartphone technology monitor covering the latest components, packaging, and silicon chip choices of smartphone makers. – Performed by System Plus Consulting

Related reports:

- Fan-Out WLP and PLP Applications and Technologies 2021
- 5G Packaging Trends for Smartphones 2021
- Fan-Out Packaging Processes Comparison 2020
- HiSilicon Hi1382 Coherent Processor with ASE's FOCoS
- Advanced System-in-Package Technology in Apple's AirPods Pro

About Yole Développement

Founded in 1998, Yole Développement (Yole) has grown to become a group of companies providing marketing, technology and strategy consulting, media and corporate finance services, reverse engineering and reverse costing

services and well as IP and patent analysis. With a strong focus on emerging applications using silicon and/or micro manufacturing, the Yole group of companies has expanded to include more than 80 collaborators worldwide… More

About System Plus Consulting

System Plus Consulting specializes in the cost analysis of electronics, from semiconductor devices to electronic systems. Created more than 20 years ago, System Plus Consulting has developed a complete range of services, costing tools and reports to deliver in-depth production cost studies and estimate the objective selling price of a product… More

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