Press Release
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LYON, France

High-End performance packaging: what are the impacts of the big players on the supply chain?[1]

OUTLINE:

- Market forecasts:
  The high-end packaging market size will reach more than US$4.7 billion by 2025.
  The high-end packaging market CAGR[2] $_{2019\text{-}2025}$ is 32%.
  The biggest market today is related to telecom and infrastructure applications.
  The most important growths, between 2019 and 2025, will be due to both market segments: mobile & consumer and automotive & mobility.
  They represent 60% and 88% market shares respectively.
- Supply chain:
  Companies of different business models including foundry, IDM[3] and OSAT[4] are competing.
  Intel Foveros™ and TSMC 3D SoIC™ are competing head-to-head. How will Samsung react?
  The barrier to entry into High-end Packaging supply chain is increasingly high with major players disrupting Advanced Packaging domain with FE[5] capabilities.

"High-end Packaging technology options are increasingly rich and ground-breaking. WLPs[6] are changing the standard of FE/BE[7] supply chain." asserts **Favier Shoo, Team Lead Analyst, Packaging at Yole Développement (Yole).**

A middle zone between FE and BE, where bumping and packaging can be executed on the wafer-level, can be reached by OSATs, WLP houses and IDMs.

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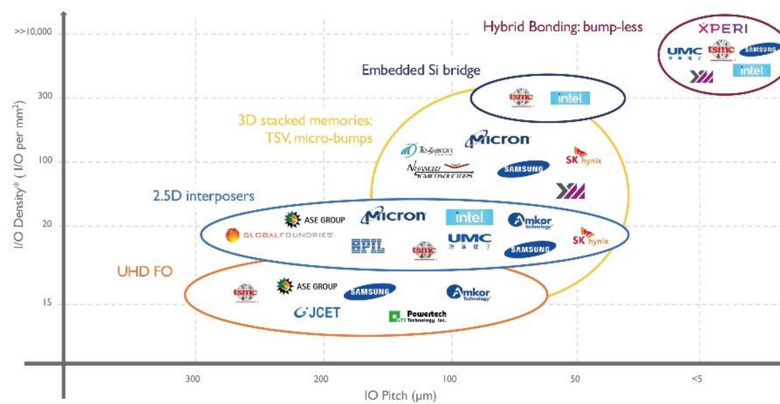
[1] Extracted from:
High-End Performance Packaging: 3D/2.5D Integration report, Yole Développement, 2020
Intel Foveros 3D Packaging Technology, System Plus Consulting, 2020
[2] CAGR: Compound Annual Growth Rate
[3] IDM: Integrated Device Manufacturers
[4] OSAT: Outsourced Semiconductor Assembly and Test companies
[5] FE: Front-End
[6] WLP: Wafer Level Packages
[7] BE: Back-End

In this context, Yole investigates disruptive technologies and related markets in depth, to point out the latest innovations and underline the business opportunities.
In this regard, the High-End Performance Packaging: 3D/2.5D Integration report presents a comprehensive overview of the high-end technologies, classified as high-end performance packaging. According to Yole's advanced packaging analysts, high-end performance packaging is defined as a forefront packaging technology, which value-adds device performance with high IO density (≥16/mm2) and fine IO Pitch (≤130µm). Yole's report identifies and analyzes the key market drivers, benefits and challenges of high-end performance packaging technologies by application. With a detailed description of each technologies, their trends and related roadmaps, this study proposes an overview of the supply chain and analyzes the competitive landscape. In addition, this report provides detailed market figures and estimates future trends. What is the status of the high-end performance packaging industry? What are the economic and technological challenges? What are the key drivers? And who are the major key glass material suppliers?
Yole presents today its vision of the high-end performance packaging industry.

Mapping of high-end packaging players based on technology

(Source: High-End Performance Packaging: 3D/2.5D Integration 2020 report, Yole Développement, 2020)



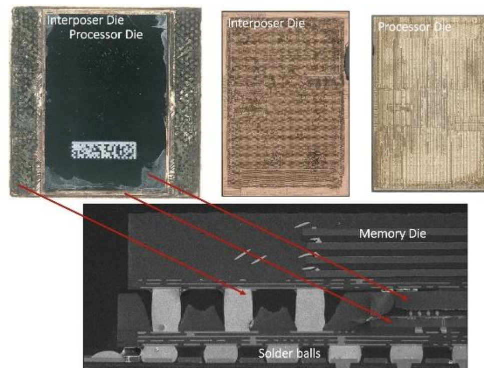
As analyzed by Yole's team in the High-End Performance Packaging: 3D/2.5D Integration report, big players like Intel, TSMC and Samsung have successfully tapped into the advanced packaging market's growth. They have achieved faster time to-market than OSATs for high-end performance packaging, at historically unprecedented scale. This strategy of big players poses a direct, formidable threat to OSATs.
Big players have both FE and BE capabilities. As a foundry, TSMC can be fundamentally focused on just FE and BE hence the new focus on 3D SoIC. So TSMC can make decisions quickly and follow through its strategy effectively. Intel has been actively promoting and commercializing its high-end packaging technologies like Foveros, EMIB and hybrid bonding for future roadmap. Intel's Foveros is a direct challenge with TSMC's CoWoS. In this regard, Yole

Développement's partner, System Plus Consulting, released the Intel Foveros 3D Packaging Technology report.

According to **Stéphane Elisabeth, PhD, Senior Technology and Cost Analyst at System Plus Consulting, part of Yole Développement (Yole):** *"Intel has developed several interconnect technologies to enable heterogenous integration using chiplets. An early glimpse of the technology enablers was seen in 2018 on an Intel processor, then called EMiB[8]. Today, Intel shows another way to interconnect dies in processor using an active interposer and Foveros technology".*

Disassembly and Cross-Section of the 3D Stacking package technology from Intel

(Source: Intel Foveros 3D Packaging Technology report, System Plus Consulting, 2020)



Hybrid Technology with Package-on-Package and Face-to-Face i.e. Foveros on Active Interposer using TSV via-middle.

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Although Samsung is leading TSV for HBM, it is not actively promoting logic 2.5D Interposers. Samsung and Intel need to ensure there is agreement from its design group all the way to system department. Any form of change is restricted by many locked-in legacies that slow down the progression for them to achieve a leading position in advanced packaging, which is typically viewed as risky and low priority.

Within high-end packaging, OSATs' business is being cannibalized by foundries and IDMs.

Moving forward, the fabless model may become more attractive thanks to cutting-edge turnkey services, such as the latest silicon node manufacturing technology coupled with advanced packaging. Fabless companies and design houses are looking to optimized packages for value for-money, especially for high-end applications. If big players can provide both quality and cost benefits, then OSATs may have to stay defensive in the existing packaging domain.

All year long, Yole Développement publishes numerous reports and monitors. In addition, experts realize various key presentations and organize key conferences.

[8] EMiB: Embedded Multi-die interconnect Bridge

Press Release

Make sure to be aware of the latest news coming from the industry and get an overview of our activities, including interviews with leading companies and more on i-Micronews. Stay tuned!

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About our analysts

Favier Shoo is a Team Lead Analyst in the Packaging team within Semiconductor, Memory and Computing Division at Yole Développement (Yole), part of Yole Group of Companies. Based in Singapore, Favier manages an international team and develops the technical expertise and market know-how within the team. Favier also focuses on the production of technology & market reports, conducts strategic consulting and custom studies. As an acknowledged professional in the semiconductor packaging market space, Favier is regularly engaged in international conferences, with presentations, keynotes, and panel review sessions. During 7 years at Applied Materials as a Customer Application Technologist in the advanced packaging field, Favier developed an in-depth understanding of the supply chain and core business values. Prior to that, Favier worked at REC Solar as a Manufacturing Engineer to maximize production. Favier holds a Bachelor's in Materials Engineering (Hons) and a Minor in Entrepreneurship from Nanyang Technological University (NTU) (Singapore). Favier was also the co-founder of a startup company where he formulated business goals, revenue models and marketing plans.

Stéphane Elisabeth, PhD is Senior Technology and Cost Analyst at System Plus Consulting, part of Yole Développement (Yole). Stéphane regularly works on numerous reverse engineering and costing reports while also managing custom projects in the RF electronics and advanced packaging fields. His mission at System Plus Consulting is to provide an in-depth understanding of the technologies selected by the leading semiconductor companies as well as the ecosystem around a device. In this context, Stéphane is leading a strategic watch to identify the latest innovative devices and collaborates closely with System Plus Consulting's laboratory to analyze devices or components. His aim is to reveal the link between functionality and the technical choice made by the device maker. Based on the identification of each process step and process flow, our analysts can then provide an accurate evaluation of the manufacturing cost. His significant industrial and technical knowledge allows him also to update internal simulation tools developed by System Plus Consulting's experts. In addition, Stéphane supports the development of RF electronics activities through key customer projects, including presentation of their results. Prior to this collaboration with System Plus Consulting, Stéphane worked on projects in partnership with THALES for the development of innovative hybrid RF circuits. He also regularly publishes articles and interviews within key RF electronics and packaging magazines. Stéphane holds an engineering degree in electronics and numerical technology (Université de Nantes, France) as well as a PhD. in Materials for Microelectronics (Université de Nantes, France).

About the reports

High-End Performance Packaging: 3D/2.5D Integration

Intel Foveros and TSMC 3D SoIC are competing head-to-head for High-End Packaging - how will Samsung react? – Performed by Yole Développement

Companies cited:

ADI, AMD, Amkor, Annapurna/Amazon, arm, ASE, Atmel, Broadcom/Avago, Broadpak, CEA-Leti, Cerebras, Cisco, Cray, Cypress, eSilicon, Facebook, Fraunhofer IZM, Freescale, Fujitsu, GlobalFoundries, Gloway, Google, Hitachi, HLMC, Huawei, Ibiden, IBM, IME, IMEC, Infineon Technologies, Intel, JCET, Juniper Networks, Kyocera, Micron, Mitsubishi, Nhanced, Nvidia and more…

Intel Foveros 3D Packaging Technology

Intel Core i5-L16G7: the first utilisation of Intel's Foveros Technology with Package-on-Package configuration in a consumer product. – Performed by System Plus Consulting

Related reports

- Status of the Advanced Packaging Industry
- Advanced Packaging Quarterly Market Monitor, Q3, 2020
- (x)PU: High-End CPU and GPU for Datacenter Applications 2020

About Yole Développement

Founded in 1998, Yole Développement (Yole) has grown to become a group of companies providing marketing, technology and strategy consulting, media and corporate finance services, reverse engineering and reverse costing

services and well as IP and patent analysis. With a strong focus on emerging applications using silicon and/or micro manufacturing, the Yole group of companies has expanded to include more than 80 collaborators worldwide… More

About System Plus Consulting

System Plus Consulting specializes in the cost analysis of electronics, from semiconductor devices to electronic systems. Created more than 20 years ago, System Plus Consulting has developed a complete range of services, costing tools and reports to deliver in-depth production cost studies and estimate the objective selling price of a product… More

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