Press Release

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LYON, France

Memory, CIS, and power electronics are driving the wafer thinning equipment market, before a new wave of innovation by 2025[1]

OUTLINES:

- Demand for thinned wafers is growing considerably: to follow the miniaturization trends while improving the performances of the devices, semiconductor substrates are thinned down with final thicknesses in the tens of µm.
- Yole Développement announces a more than 5% CAGR[2][3] between 2019 and 2025 to reach more than 135 million thinned wafers at the end of the period.
- The market is mainly pushed by memory, CIS[4] and power SiC[5] components as well as LED and laser diodes.
- The thinning equipment market is dominated by the two major grinding & CMP equipment suppliers, DISCO, ACCRETECH. They are followed by Revasum and Ebara.

"The demand for thinned wafers continues to increase owing to miniaturization associated with greater performance driven by a wide range of applications, such as stacked packages within mobile devices and other consumer products," explains **Amandine Pizzagalli, Technology & Market Analyst at Yole Développement (Yole).** According to the new Thinning Equipment Technology & Market Trends for Semiconductor Devices report released by Yole today, the thinned wafer market is showing a significant growth from 100 million to more than 135 million thinned wafers.

In parallel, the market research and strategy consulting company announces almost10% CAGR during the same period for the overall thinning equipment market. Analysts deeply focused on the technical issues and market trends. According Yole's semiconductor manufacturing team, this industry was worth almost US$461 million in 2019 and will exceed almost US$792 million by 2025 mainly generated by memory, CIS and power SiC components as well as LED and laser diodes.

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[1] Extracted from Thinning Equipment Technology & Market Trends for Semiconductor Devices report, Yole Développement, 2020
[2] In volume
[3] CAGR : Compound Annual Growth Rate
[4] CIS : CMOS Image Sensors
[5] SiC : Silicon Carbide

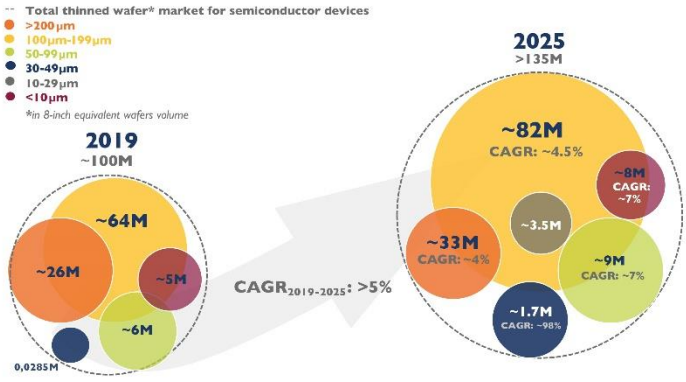
The Thinning Equipment Technology & Market Trends for Semiconductor Devices report is a comprehensive analysis of the major applications currently using thinning methods. It details attractive applications as well as the key benefits and added value of thinning technology in the semiconductor field. Yole's analysts deliver today a relevant study of this industry with accurate market forecasts (breakdown by device type, by substrate type and by equipment technology. The competitive landscape including the identification of the key players, their market positioning and strategy is also well described in this new semiconductor manufacturing report.

"With this new report, our aim was to cover the different equipment used for thinning down and polish the semiconductor wafer substrates," explains **Gaël Giusti, PhD., Technology & Market Analyst at Yole.** *"The scope was focused on the back-end part for semiconductor devices industry. We also added thin film layers market segment. Moreover, this report was an opportunity to point out the market drivers as well as the limitations of each technology".*

What is the status of the thinning technologies today? Behind the existing and emerging technologies, who are the main companies involved? With a strong growth between 2019 and 2025 in volume and a new wave of innovations after 2025, how will each market segment evolve? Yole's semiconductor manufacturing analysts are pleased to deliver today a snapshot of the thinning technologies and related applications.

Thinned wafer market volume: 2019-2025 breakdown by thickness range

(Source: Thinning Equipment Technology and Market Trends for Semiconductor Devices 2020 report, Yole Développement, 2020)



Today, most semiconductor wafers are thinned down to a range of 100 µm-200 µm especially when it comes to memory, CIS and power applications.

However, some silicon wafers are thinned down well below 100 µm in HVM[6], including some 3D stacked memory devices, CIS and power devices. The total memory architecture thickness varies typically from 50 µm to 400 µm depending on the manufacturer and the packaging

[6] HVM : High Volume Manufacturing

technology. For instance, standard memory, like DRAM[7] or 2D NAND, uses silicon wafers that are thicker than 200 µm, while 3D stacked DRAM keeps moving downward, from 50 µm to 30 µm thick silicon substrates by 2025. Incidentally, the 30 µm to 50 µm thickness range is the one in which the largest number of thinned wafers is expected by 2025.

Meanwhile, BSI[8] CIS wafers are thinned down below 10 µm thickness and are today the thinnest wafers across all semiconductor applications.

"The thickness of power devices depends on applied voltage as well as semiconductor substrate type," explains Amandine Pizzagalli from Yole. And she adds: *"From a wafer substrate point of view, Si-based MOSFETs involve wafer thickness of around 50 µm to 55 µm on 300 mm diameter wafers in HVM with a trend towards thinning down to 30 µm. Wafer thicknesses for SiC-based devices are rarely lower than 200 µm even though thickness reduction is expected to go down to 100 µm/110 µm in the next few years."*

In parallel, typical wafer thickness for MEMS[9] sensors is today in a range of 200 µm to 350 µm, especially for inertial MEMS.

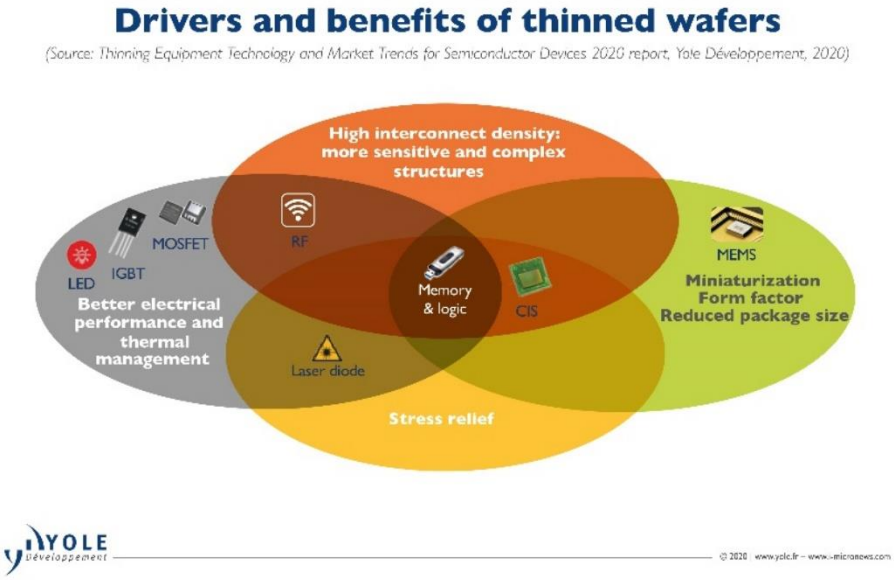
At the end, RF wafers devices are in the range of 140 µm and 200 µm and are opposite to every other the semiconductor devices in terms of thickness reduction. RF device wafers are getting thicker, with the thickness depending on whether wire bonding or flip-chip packaging will be more widely adopted by the industry.

"Myriad thinning technology steps are applied for the fabrication of semiconductor devices," comments Gaël Giusti from Yole. At the back-end wafer stage, thinning methods are employed for thinning down the wafers and sometimes even removing the substrate, for LEDs on silicon for example. Although there are similar and common drivers for thinning's applicability in semiconductor applications, the reasons for using such techniques differ from one device to another and depend on the end-applications. *"This is a critical point as it demonstrates that a change in architecture or a disruptive technology with potential large volumes involved can have a tremendous impact on the wafer thinning equipment market,"* explains Gaël Giusti.

The microLED market, should it take off and should it use back thinning technologies, could give a significant boost both to wafer-starts and to the corresponding equipment market.

The same can be said for CIS, 3D sensing applications or a widespread shift to SiP[10] technology. As of today and in the case of MEMS devices, such components are typically composed of a stack of a sensor element wafer, a cap and an ASIC[11]. All three wafers must be thinned to reduce the size of the device.

[7] DRAM : Dynamic Random Access Memory
[8] BSI : Back-Side Illumination
[9] MEMS : Micro Electro Mechanical System
[10] SiP : System in Package
[11] ASIC : Application Specific Integrated Circuit



With respect to power devices, thin wafers are needed here since reduced thickness lowers on resistance, improves current carrying capability and minimizes power consumption.
On the other hand, CMOS image sensor wafers are thinned down for TSV packaging where thinning is needed to achieve a very small form factor. BSI with extreme thinning below 10 µm enhances light sensitivity, while hybrid stack and triple stack architectures are pushing the boundaries further.
Traditional LED fabrication also requires a thinning or a removal step at the back-end for miniaturization and easier dicing/singulation. Laser diode requirements are much less stringent but the emergence of high-power VCSELs demands much thinner wafers for enhanced heat management. In the case of memory devices, further thickness reduction is driven by the need to maximize memory capacity of single packages, improved data transfer rates as well as power consumption mostly fueled by mobile applications.

All year long, Yole Développement publishes numerous semiconductor equipment and materials reports. Yole's experts also propose key presentations through a powerful program of events. Discover them on i-Micronews. *Stay tuned!*

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About our analysts

Amandine Pizzagalli is a Technology & Market Analyst, Equipment & Materials - Semiconductor Manufacturing, at Yole Développement (Yole). Amandine is part of the development of the Semiconductor & Software division of Yole, producing reports and custom consulting projects. She is in charge of comprehensive analyses focused on semiconductor equipment, materials and manufacturing processes.
Previously, Amandine worked as Process Engineer on CVD and ALD processes for semiconductor applications at Air Liquide. Amandine was based in Japan for one year to manage these projects.
She has spoken in numerous international conferences and has authored or co-authored more than 10 papers.
Amandine holds an international MBA from IAE Lyon, School of Management, France, and an electronic engineering master degree from the engineering school, CPE Lyon, France, with an added degree, focusing on semiconductor manufacturing technology, from KTH Royal Institute of Technology, Sweden

Gaël Giusti, PhD., is a Technology & Market Analyst specializing in Semiconductor Manufacturing and Equipment & Materials at Yole Développement (Yole). As part of the Semiconductor & Software division at Yole, Gaël's expertise is focused on thin film growth and related applications, equipment, materials and manufacturing processes. He is involved daily in the production of technology & market reports and custom consulting projects.
Prior to Yole, Gaël served as a R&D engineer at Sil'Tronix Silicon Technologies for 5 years where he was in charge of upscaling a CVD process to develop epitaxial AlN thin film on sapphire for RF applications. He also worked on transparent conducting thin films for optoelectronics applications as a post-doctoral researcher at LMGP (Grenoble, France).
Gaël holds a master's degree from ENSICAEN (Caen, France) as well as a PhD in Materials Science from the University of Birmingham (UK).

About the report

Thinning Equipment Technology & Market Trends for Semiconductor Devices

The demand for thinned wafers continues to increase owing to miniaturization associated with greater performance driven by a wide range of applications, such as stacked packages within mobile devices and other consumer products… - Performed by Yole Développement

Companies cited

3M, Accretech, Allied High-Tech Products, Anji, Applied Materials, Baikowski, Buehler, Cabot Microelectronics, Chemical, Disco, Dongjin Semichem, DuPont, Ebara, Engis, Evonik, Ferro, Fujimi, Fujifilm, Fuso Chemical, Hitachi Chemical, JSR Corporation, KC Tech, LAM PLAN, Logitech, microdiamant, Nissan Chemical, Nitta, and many more...

About Yole Développement

Founded in 1998, Yole Développement (Yole) has grown to become a group of companies providing marketing, technology and strategy consulting, media and corporate finance services, reverse engineering and reverse costing services and well as IP and patent analysis.
With a strong focus on emerging applications using silicon and/or micro manufacturing, the Yole group of companies has expanded to include more than 80 collaborators worldwide covering MEMS & Sensors - Imaging - Medical Technologies - Compound Semiconductors - RF Electronics – Solid State Lighting - Displays - Photonics - Power Electronics - Batteries & Energy Management - Advanced Packaging - Semiconductor Manufacturing - Software & Computing - Memory and more...
The market research, technology and strategy consulting company Yole Développement, along with its partners System Plus Consulting, PISEO and KnowMade, support industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to grow their business… More

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