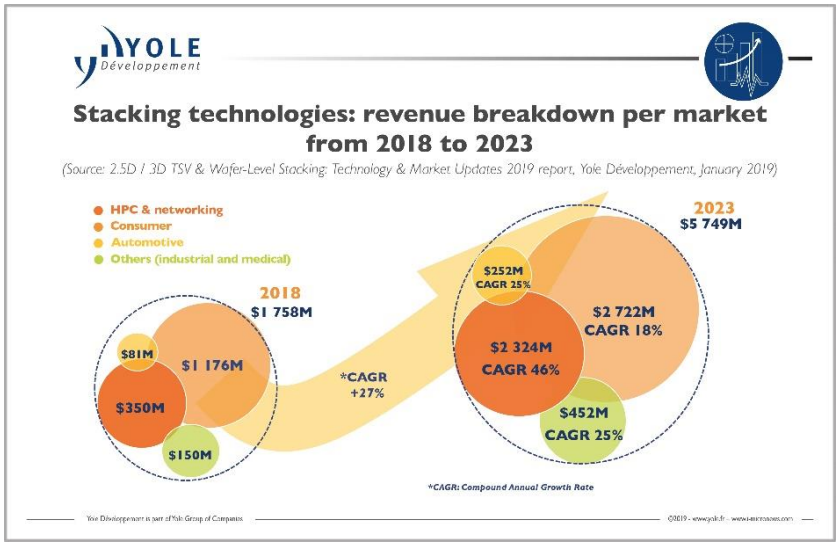
FOR IMMEDIATE RELEASE:

High performance computing, artificial intelligence and datacenter: the 2.5D & 3D stacking technologies playground

Extracted from: 2.5D / 3D TSV & Wafer-Level Stacking: Technology & Market Updates report, 2019 edition - Yole Développement | Intel's Embedded Multi-Die Interconnect Bridge (EMIB) report, 2018 edition, System Plus Consulting

Online webcast powered by SEMI – Recorded version: Stacking: the future for packaging technologies!

LYON, France – February 7, 2019: *"2.5D and 3D stacking technologies are the only solution that meet the required performance of applications like AI[1] and datacenter as for today"*, confirms **Mario Ibrahim, Technology & Market Analyst from Yole Développement (Yole).** Stacking technologies are used in a variety of hardware, including 3D stacked memory, GPU[2], FPGA[3], and CIS[4], are intended for the high/mid and low-end market segments.



Hardware like HBM and CIS comprise the majority of TSV's[5] revenue. The overall stacking technologies market will exceed US$5.5 billion in 2023 with a CAGR of 27%, announces Yole it its latest advanced packaging report, 2.5D / 3D TSV & Wafer Level Stacking: Technology & Market Updates report. As for today, the consumer market is the biggest contributor, with over 65% market share. But this, paradoxically, doesn't mean that consumer is the driver for these technologies. In reality, HPC is the real driver for stacking technologies and will exhibit the fastest growth up to 2023, with market share doubling from 20% in 2018 to 40% in 2023. In terms of packaging revenue, this equates to a more than 6x increase from 2018's revenue. Consequently, the consumer market's share will decrease. Other

[1] AI : Artificial Intelligence
[2] GPU : Graphics Processing Unit
[3] FPGA : Field-Programmable Gate Array
[4] CIS : CMOS Image Sensor
[5] TSV: Through Silicon Via

markets like automotive, medical, and industrial will maintain their current market share.

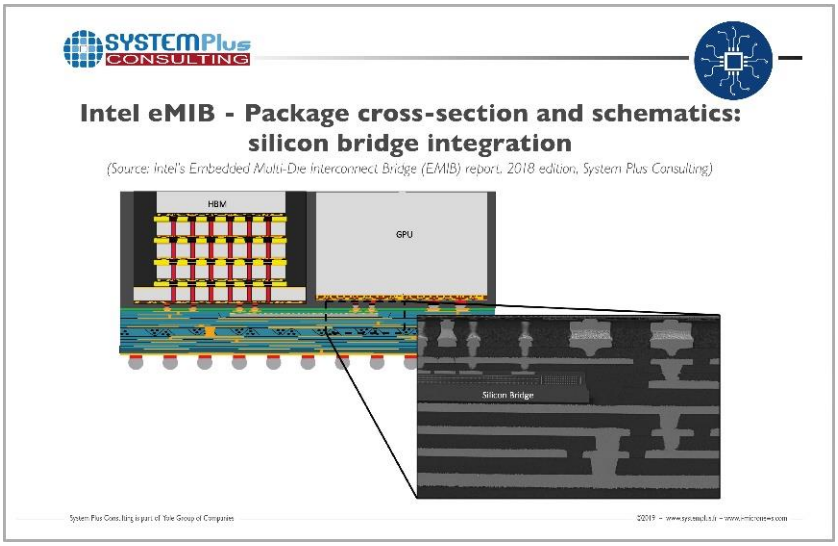
Yole and System Plus Consulting, both part of Yole Group of Companies propose today two dedicated reports that explore the 2.5D heterogeneous and 3D wafer-level stacking technologies. The 2.5D / 3D TSV & Wafer-Level Stacking: Technology & Market Updates report from Yole outlines three stacking technologies, TSV, 3D SoC[6], and hybrid bonding and provides a comprehensive overview of the different market segments including industry trends, market forecasts and technology trends.

In parallel, under its Intel's EMIB[7] report, System Plus Consulting dives deeply into Intel's integration know-how with the world's first on-package CPU[8] and GPU with high bandwidth memory. The reverse engineering & costing company full analyzed the eight generation of Intel core i7 processor. Intel's processor features a CPU, a discrete GPU and HBM2[9] on the same package. The GPU has a 4GB high bandwidth cache assembled from one 4-Hi HBM2 stack of four DRAM dies, giving almost 200GB/s of bandwidth…

2.5D heterogeneous and 3D wafer-level stacking are clearly reshaping the packaging landscape… System Plus Consulting and Yole invites you to get a deep understanding of the latest technical innovations, the targeted markets and related challenges.

For today's high-end market segment, the most popular 2.5D and 3D integration technologies on the market are based on TSV for 3D stacked memory, and TSV interposer for heterogeneous stacking.

CoWos[10] technology is already widely used for HPC applications, and new TSV technologies will hit the market in 2019. As an example, Foveros from Intel is based on "active" TSV interposer and 3D SoC technology, with hybrid bonding and TSV interconnections (potentially). Foveros from Intel shows, although TSV is being challenged by non-TSV technologies, companies still have faith in it.



In parallel, Yole's analysts also underline the emergence of TSV-less technologies in the market. Such innovations can

[6] SoC : System-on-Chip
[7] EMIB: Embedded Multi-Die Interconnect Bridge
[8] CPU : Central Processing Unit
[9] HBM2 : second generation high bandwidth memory
[10] CoWos : Chip-on-Wafer-on-Substrate

be placed into two groups: "with substrate" and "embedded in substrate".

EMIB technology, already commercialized, is part of the embedded-insubstrate group, where the silicon bridge is deep seating in the substrate. Within System Plus Consulting EMIB report, **Stéphane Elisabeth, Expert, Cost Analyst at System Plus Consulting** underlines Intel's expertise: *"In the past few years, needs for high DRAM bandwidth has led to increasing investments to develop innovative packages. Localized high density interconnects devices between two or more dies has so been investigated. Objective was clearly to provide a higher bandwidth signal in order to open up new opportunities for heterogeneous on-package integration."*…Typical proposed devices are today glass, organic or silicon interposers. And Intel has developed its own approach with EMIB solution, which offers simpler integration.

With-substrate technologies are also used as alternatives to TSV. For example InFO on substrate is widely used in Apple's processors. Also, RDL[11] interposer technology is currently being developed and will hit the market by 2020. Last but not least, FOCoS[12] was developed and commercialized in 2016, but seems to be lacking orders.

Hybrid bonding can bridge the two main categories (with TSV/without TSV). This technology's particularity is that it can be simultaneously TSV challenger and teammate. Since 2016 it has been commonly used in smartphones' CIS, and in the near future it will integrate the high-end market segment for memory and 2.5D as an interconnection solution…

Invited by SEMI for a dedicated advanced packaging webcast last month, Yole proposed a valuable presentation focused on the 3D stacking technologies status and the related market segments. Mario Ibrahim from Yole had the opportunity to point out the technology evolution and market opportunities.

The recorded version is now available: click Stacking: the future for packaging technologies! – Webcast.

[11] RDL: redistribution layer
[12] FOCoS : Fan Out Chip on Substrate

ABOUT THE REPORTS:

2.5D / 3D TSV & Wafer-Level Stacking: Technology & Market Updates 2019

2.5D heterogeneous and 3D wafer-level stacking are reshaping the packaging landscape. – Produced by Yole Développement (Yole).

Companies cited in the report:

Alchip, Aledia, Alibaba, Amazon, AMD, Amkor, AMS, ANPEC, Apple, ASE, ASUS, Atos, Audi, Avago, Baidu, Bosch, Bitmain, BitFury, Broadcom, Canaan, Carsem, Cisco, Cray, DARPA, EBANG, EMmicroelectronic, EPworks, Facebook, Faraday, Fingerprints, Foxconn …Full list

Author:

Mario Ibrahim is a member of the Semiconductor & Software division at Yole Développement (Yole), working as a Technology & Market Analyst for advanced packaging. Mario develops technology & market reports and produces custom consulting studies. He is also deeply involved in test activity business development within the division. Prior to Yole, Mario specialized in test activity development for LEDs at Aledia. He also headed several R&D advanced packaging programs. During his five-year stay at Aledia, Mario developed strong technical and managerial expertise in different semiconductor fields.

Mario holds an Electronics Engineering degree from Polytech Grenoble (France). He apprenticed for three years in the Imaging division of STMicroelectronics Grenoble, where he contributed to the testing and benchmarking of automation advancements within the test & validation team.

Intel's Embedded Multi-Die Interconnect Bridge (EMIB)

First consumer application in the Intel Core 8th Generation i7-8809G, the world's first On-Package CPU and GPU with High Bandwidth Memory. – Produced by System Plus Consulting.

Authors:

Dr. Stéphane Elisabeth has joined System Plus Consulting's team in 2016. He has a deep knowledge of Materials characterizations and Electronicssystems. He holds an Engineering Degree in Electronics and Numerical Technology, and a PhD in Materials for Microelectronics.

Véronique Le Troadec has joined System Plus Consulting as a laboratory engineer. Coming from Atmel Nantes, she has extensive knowledge in failure analysis of components and in deprocessing of integrated circuits

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System Plus Consulting specializes in the cost analysis of electronics, from semiconductor devices to electronic systems. Created more than 20 years ago, System Plus Consulting has developed a complete range of services, costing tools and reports to deliver in-depth production cost studies and estimate the objective selling price of a product.

System Plus Consulting engineers are experts in Integrated Circuits - Power Devices & Modules - MEMS & Sensors - Photonics – LED - Imaging – Display - Packaging - Electronic Boards & Systems. Through hundreds of analyses performed each year, System Plus Consulting offers deep added-value reports to help its customers understand their production processes and determine production costs. Based on System Plus Consulting's results, manufacturers are able to compare their production costs to those of competitors. System Plus Consulting is a sister company of Yole Développement. More info on www.systemplus.fr and on LinkedIn and Twitter.

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The "More than Moore" market research, technology and strategy consulting company Yole Développement, along with its partners System Plus Consulting, PISEO and KnowMade, support industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to grow their business. . For more information, visit www.yole.fr and follow Yole on LinkedIn and Twitter.

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