PRESS RELEASE

Embedded Wafer-Level-Packages – 2010 Report
Both Fan-Out WLP / Chip Embedding in Substrate technologies covered

Yole presents its new report to understand and prepare for the next generations of IC packaging & substrate assembly waves!

June 10th, Lyon, France – Yole Développement announce the imminent release of its latest research study about Embedded Wafer-Level-Packages, covering the industry status in the commercialization of both Fan-Out WLP and Chip Embedding in Substrate technologies.

Historically, embedded IC package technology is not new at all: several players such as Freescale with its RCP, Infineon with its eWLB and Ibiden for die embedding into PCB laminated substrates have developed dedicated technologies and process IP in this area for years. Benefits of embedded package integration include miniaturization, improvement of electrical and thermal performance, cost reduction and simplification of logistic for OEMs.

“Things are moving really fast at the moment as this year, we see both Fan-out wafer level packaging and chip embedding into PCB laminate infrastructures emerging at the same time, ramping to high volume production.” says J. Baron, Technology & Marketing Analyst at Yole Développement.
Fan-Out WLP technology is emerging on both 200mm / 300mm infrastructures

Infineon is having a great success with its proprietary eWLB technology: the first FO-WLP wafers are mass produced on 200mm both at Infineon, STATS ChipPAC and ASE since 2009.

Indeed, Fan-Out WLP is extending the general concept of Wafer Scale Packaging to new application categories, especially the ones with higher pin-counts and larger chip size such as wireless communication ICs. First embedded package products based on eWLB have been identified within LGE and Nokia handsets.

This year, a few additional players are even more aggressive in putting further capacity for eWLB manufacturing as both STATS ChipPAC and NANIUM are at the moment ramping-up their facilities for manufacturing the first generation eWLB on 300mm reconfigured wafers. Other packaging houses such as SPI, Amkor, UTAC, ACET and others are also on the point to announce the start of their own Fan-out wafer level packaging operations.

Embedded die package technology to expand fast from niche to high volume markets

At the same time, embedded die package technology has made a lot of progress on its side. Based on PCB laminate infrastructure, chip embedding technology is actually on the way to catch a relatively important portion of the actual WLCSP packaging business as it does leverage the existing WLP/RDL infrastructure already established worldwide: indeed, most of WLCSP die applications are “embedded ready”, so to realize the full benefits of this “WLCSP to Embedded die” conversion, only a few extra manufacturing steps are missing like the realization of thin copper plating process, extreme wafer thinning down to 50μm, thin dies handling and dicing.

Electrical performance, testing and manufacturing yields are still major issues and showstoppers for chip embedding technology to move forward. Therefore, initial volume markets for embedded packages will be rather small, low pin-counts analog type of applications such as integrated passive devices (IPD), RFID and power components that are at the moment under qualification for mass production before the end of this year already.

Generally speaking, Yole Développement believe that the winning situation for embedded die packages can be met for company partnerships able to cross-over the traditional packaging, assembly and test supply chain. A good example would be to put together a leading analog IC player (such as TI, Maxim IC, NXP or ST) with a WLP/RDL partner (such as FCI, Casio Micronics, NEPES, etc...) together with a PCB integrator player (such as Imbera / Daeduck, Ibiden, AT&S, Taiyo Yuden or SEMCO). This type of emerging partnerships are absolutely necessary in order to standardize the embedded package technology and to leverage an entire new packaging infrastructure based on low-cost, panel size PCB manufacturing techniques.
FOWLP versus Chip Embedding: competing technologies and infrastructures?

Today, embedded die and Fan-Out WLP technologies are not competing at all. Indeed, these two emerging semiconductor packaging techniques are targeting very different applications initially: the chip embedding technology is looking for replacement of low cost, low pin-counts WLCSP / SOT / QFN / LGA family package applications while FOWLP technology is rather targeting the direct replacement of higher I/Os (> 120 pins) BGA package applications. However, in the long term, with standardization and through further technology improvements towards higher yield, better electrical performance, lower profile, better testability and smaller pitch features, Fan-out WLP and Embedded die technology could seriously compete in the fast growing 3D Packaging market space as they will both enable the construction of ever more complex, larger SiP modules with different active and passive functions, all connected on both sides of the active substrate... So Fan-out WLP and chip embedding into PCB laminates are just two additional key pieces of the widening tool-box for 3D Packaging!

###

About the Authors of this new research study:

Jean-Marc Yannou recently joined Yole Développement as technology and market expert in the fields of advanced packaging and Integrated Passive Devices. He has 15-years of experience in the semiconductor industry. He worked for Texas Instruments and Philips (then NXP semiconductors) where he served as “Innovation Manager” for System-in-Package technologies

Jérôme Baron is leading the MEMS and Advanced Packaging market research at Yole Développement. He has been involved in the technology analysis of the 3D packaging market evolution at device, equipment and material supplier levels. He was granted a Master of Science degree in Micro & Nanotechnologies from the National Institute of Applied Sciences in Lyon, France.

Wafer Level Packaging report

Catalogue price: Euros 3,990.00 (single user license)
Publication date: July 2010
For special offers and the price in dollars, please contact David Jourdan (jourdan@yole.fr or +33 472 83 01 95)

Other Advanced Packaging reports

- **IPD Market Report 2009, Technologies, Applications, Markets & Players**: First complete study on Thin Film Integrated Passive & Active Devices. It exhaustively lists the existing and upcoming technologies and applications for IPDs. The report not only describes the market and the associated technologies deep inside the applications, but it also provides a broad overview of the thin-film IPD market and its forthcoming growth opportunities.

- **Memory Applications, Packaging & Integration Trends 2009**: New study aims at answering the following questions: What are the end applications driving the use of 3-D integrated memories? Who are the key players doing it? How will it happen? When will the market ramp up? What is the impact of the current economic turmoil? How big is this 3-D memory market going to be and at which conditions? How will 3D TSV technologies boost new applications and drive the growth of flash and DRAM market?
About Yole Développement in the Advanced Packaging industry

From technologies to market, we help our clients to develop their business in the Advanced Packaging industry. Our commitment is to facilitate market access for innovative technologies, equipment and materials.

We study comprehensive technology, market and value chain analysis of the semiconductor packaging industry throughout the many available packaging platforms, from equipment and materials down to the end-user applications.

Yole Développement works worldwide with the key industrial companies, R&D institutes and investors in order to help them to understand the markets and technology trends. We take into account the complete value chain in our analysis, from materials and equipment business to device and system manufacturers and final users.

Yole is working with its customers at every stages of the development, from R&D to industrial development, from initial ideas to market launch of finished products.

Contacts
Yole Développement
45 Rue Ste Geneviève, 69006 Lyon, France
Tel : +33 (0) 472 83 01 80
Fax : +33 (0) 472 83 01 83
www.yole.fr

About Yole Développement, please contact Jean Christophe Eloy, CEO, eloy@yole.fr
About this report and Advanced Packaging activity, Jérôme Baron (baron@yole.fr) and Jean-Marc Yannou (yannou@yole.fr)