Fan-in WLP manufacturing capacities are full and more volume is required ... Yole announces its new advanced packaging analysis

**Fan-in Wafer Level Packaging: Market and Technology Trends report**

**LYON, France – May 28, 2015** – “The semiconductor industry is facing a new era in which device scaling and cost reduction will not continue on the path they followed for the past few decades, with Moore’s law in its foundation”, asserts Andrej Ivankovic, Technology & Market Analyst, in the Advanced Packaging and Semiconductor Manufacturing team, at Yole Développement (Yole). Under this context, the semiconductor industry seeks further performance and functionality boosts in package level integration. Emerging packages such as fan-out wafer level packages, 2.5D/3D IC and related System-in-Package (SiP) solutions together with more conventional but upgraded flip chip BGAs aim to bridge the gap and revive the cost/performance curve. In such an environment, what is the importance of fan-in wafer level packages, the current status of the fan-in WLP industry and how will fan-in WLP market and technology evolve? ...

The “More than Moore” market research and strategy consulting company, Yole confirms its leadership in the advanced packaging industry with its new technology & market report entitled **Fan-in Wafer Level Packaging: Market & Technology Trends report**. With this new analysis, the consulting company covers a broad part of the existing and emerging advanced packaging technologies and related platforms: indeed Yole’s collection includes **Fan-Out and Embedded Die: Technologies & Market Trends** (Feb. 2015), **Equipment & Materials for 3DIC & Wafer-Level Packaging Applications** (Nov. 2014) and **3DIC & 2.5D TSV Interconnect for Advanced Packaging 2014 Business Update** (Oct. 2014) ...

**Fan-in Wafer Level Packaging: Market & Technology Trends report** provides a market overview of the fan-in Wafer Level Packaging (WLP) landscape including emerging and declining applications, forecasts until 2020, supply chain analysis and main players...

Although present for more than a decade, fan-in WLP are still on an evolutionary track increasing production and attracting new applications. Current market data indicate fan-in WLP manufacturing capacities are full and more volume is required in both 200mm and 300mm wafer sizes.
Furthermore, the “Internet of Things” (IoT) promises a wide range of new applications for which fan-in WLP would be an ideal match presenting an interesting opportunity to increase the demand further.

How will the current capacities be increased, who will take lead in investments and what is the actual range of investments needed? Currently, majority of production is still done on 200mm wafers with 300mm wafer production projected to increase. An in depth analysis addressing these questions is done in Yole’s report, including competition analysis of business models (OSAT, IDM, WLP house, foundry), their market shares and prediction of future investment.

As illustrated in Yole’s non-exhaustive map of fan-in WLP manufacturers, there are many players currently active on the market: Maxim, FlipChip, Freescale for example in the US area – ipdia, NXP, nanium, STMicroelectronics, Robert Bosch ... in Europe – And OKI, Fujitsu, nepes, Fujikura ... in Asia.

The supply chain continues to develop with new companies entering this market and new business models being established. The competitive landscape is expected to increase as well as collaborations and partnerships. The specialized wafer level packaging model, focused on fan-in and fan-out packages is emerging strong and competing with traditional OSAT leaders. Some new players are rising quickly, foundry involvement is no longer a small dent and new players from China are increasing activity on the market, bringing in a new type of competition with a strong support in capital and acquisition capabilities.

“In total, over 70 fabless and IDM companies implementing their design in fan-in WLP were identified, along with over 20 fan-in WLP manufacturing companies”, details Santoh Kumar, Senior Technology & Market research analyst, Advanced Packaging and Semiconductor Manufacturing at Yole. All details are included in Yole’s report including competitive analysis of these players. More info. on www.i-micronews.com, advanced packaging reports section.
About Fan-in Wafer Level Packaging: Market and Technology Trends report:
Rates: Euros 5,990.00 (Full report - Multi user license). For special offers and the price in dollars, please contact David Jourdan (Phone: +33 472 83 01 90).
“Fan-in Wafer Level Packaging: Market and Technology Trends” report from Yole Développement will be available on June 22, 2015.

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Andrej Ivankovic is a Technology & Market Analyst, in the Advanced Packaging and Semiconductor Manufacturing team, at Yole Développement. He holds a master’s degree in Electrical Engineering, with specialization in Industrial Electronics from the University of Zagreb, Croatia and a PhD in Mechanical Engineering from KU Leuven, Belgium. He started as an intern at ON Semiconductor performing reliability tests, failure analysis and characterization of power electronics and packages. The following 4 years he worked as a R&D engineer at IMEC Belgium on the development of 3D IC technology, focusing on electrical and thermo-mechanical issues of 3D stacking and packaging. Part of this time he also worked at GLOBALFOUNDRIES as an external researcher. He has regularly presented at international conferences authoring and co-authoring 18 papers and 1 patent.
Thibault Buisson is a member of the Advanced Packaging team at Yole Développement. He graduated from INPG with a Master of Research in Micro and Nano electronics and from Polytech’ Grenoble with an engineering degree in Material Sciences. He then joined NXP Semiconductors as R&D process engineer in the thermal treatment area to develop CMOS technology node devices from 65 to 45nm. Afterwards, he joined imec Leuven and worked for more than 5 years as process integration engineer in the field of 3D technology. During this time, he has worked on several topics from TSV to micro-bumping and stacking. He has authored or co-authored fifteen international publications in the semiconductor field.
Santosh Kumar is currently working as Senior Technology & Market Research Analyst at Yole Développement. He worked as senior R&D engineer at MK Electron Co. Ltd where he was engaged in the electronics packaging materials development and technical marketing. His main interest areas are advanced electronic packaging materials and technology including TSV and 3D packaging, modeling and simulation, reliability and material characterization, wire bonding and novel solder materials and process etc. He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 20 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

Companies cited in the report:

About Yole Développement
Founded in 1998, Yole Développement has grown to become a group of companies providing marketing, technology and strategy consulting, media and corporate finance services. With a strong focus on emerging applications using silicon and/or micro manufacturing, the Yole Développement group has expanded to include
more than 50 collaborators worldwide covering MEMS, Compound Semiconductors, LED, Image Sensors, Optoelectronics, Microfluidics & Medical, Photovoltaics, Advanced Packaging, Manufacturing, Nanomaterials and Power Electronics. The group supports industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

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