Technology innovation is driven fan-in Wafer Level Packaging adoption with more and more applications

Fan-in Wafer Level Packaging: Market and Technology Trends report

LYON, France – June 22, 2015 – According to Yole Développement’s (Yole) latest report “Fan-in Wafer Level Packaging: Market & Technology Trends”, fan-in WLP is experiencing continuous growth and attracting new applications. Indeed fan-in WLP technology confirms its presence on the semiconductor market with indisputable benefits linked to cost and form factor. Technology innovation continues and widens the sphere of possibilities of fan-in WLP solutions.

“Fan-in Wafer Level Packaging: Market & Technology Trends” report proposes a deep analysis of the fan-in WLP technology trends with a dedicated roadmap and an overview of latest technical innovations. Under this report, the “More than Moore” market research and strategy consulting company, Yole, also reviews the potential disruptions including new market drivers, infrastructure, expanding business models, new entries, competing packaging solutions... And analyzes the impact on the supply chain.

Although seemingly out of the spotlight, fan-in Wafer Level Packages (WLP) remain a highly important and constant presence with unmatchable advantages in cost and form factor. Fan-in WLP holds 16% of the total number of packages, while serving 4.4% of the wafer market at only 1.5% of the total semiconductor revenue.

“Fan-in WLP is forecasted to continue a stable growth, with a market of US$5.3B in 2014 and a CAGR between 2014 and 2020 of 7%”, explains Andrej Ivankovic, Technology & Market Analyst, in the Advanced Packaging and Semiconductor Manufacturing team, at Yole. And he adds: “The total wafer count in 300mm equivalent wafers is reaching 4 million with a projected CAGR of 8% while the unit number is found at 36 billion with a projected CAGR of 9%”. Throughout the past few years, MEMS and CMOS image sensors have been increasing their share compared to analog, mixed signal and digital ICs and are now accounting for more than 50% of the total revenue.

The leading applications by wafer demand in the analog/mixed signal/digital domain are BT+WiFi+FM combos and RF transceivers followed by PMU, audio/video codecs, DC/DC converters, ESD/EMI IPD. MEMS devices are led by digital compasses, RF filters,
accelerometers and gyroscopes. CMOS image sensors are strongly positioned in 2nd place by overall fan-in application rankings. In total 41 applications and their evolution are analyzed in more depth within Yole’s report. Yole’s data include breakdowns of MEMS, CMOS image sensors and analog, mixed signal and digital devices.

From a technology viewpoint, innovation continues in order to extend fan-in WLP capability, as summarized in Yole’s figure above.

“Current bump pitch in high volume is mostly at 0.4mm with 0.35mm already present as well. Particular effort is being made to increase the die size and I/O count” says Santosh Kumar, Senior Technology & Market research analyst, Advanced Packaging and Semiconductor Manufacturing at Yole. Max I/O count in high volume is heading above 200 and announcements have been made for high volume production up to 800 I/Os. The die size sweet spot ranges up to 7mm x 7mm with 8mm x 8mm and 9mm x 9mm qualified and ready.

Yole’s technology & market analysis contains an in-depth analysis on the outlook for bump pitch, die size, I/O count, minimum line width/space, package thickness, RDL dielectric materials, who is developing which technology and the main challenges to be overcome for the evolution of fan-in technology. Fan-in WLP is still on track of technology innovation... More info. on www.i-micronews.com, advanced packaging reports section.
**Authors:**

**Andrej Ivanovic** is a Technology & Market Analyst, in the Advanced Packaging and Semiconductor Manufacturing team, at Yole Développement. He holds a master’s degree in Electrical Engineering, with specialization in Industrial Electronics from the University of Zagreb, Croatia and a PhD in Mechanical Engineering from KU Leuven, Belgium. He started as an intern at ON Semiconductor performing reliability tests, failure analysis and characterization of power electronics and packages. The following 4 years he worked as a R&D engineer at IMEC Belgium on the development of 3D IC technology, focusing on electrical and thermo-mechanical issues of 3D stacking and packaging. Part of this time he also worked at GLOBALFOUNDRIES as an external researcher. He has regularly presented at international conferences authoring and co-authoring 18 papers and 1 patent.

**Thibault Buisson** is a member of the Advanced Packaging team at Yole Développement. He graduated from INPG with a Master of Research in Micro and Nano electronics and from Polytech’ Grenoble with an engineering degree in Material Sciences. He then joined NXP Semiconductors as R&D process engineer in the thermal treatment area to develop CMOS technology node devices from 65 to 45nm. Afterwards, he joined IMEC Leuven and worked for more than 5 years as process integration engineer in the field of 3D technology. During this time, he has worked on several topics from TSV to micro-bumping and stacking. He has authored or co-authored fifteen international publications in the semiconductor field.

**Santosh Kumar** is currently working as Senior Technology & Market Research Analyst at Yole Développement. He worked as senior R&D engineer at MK Electron Co. Ltd where he was engaged in the electronics packaging materials development and technical marketing. His main interest areas are advanced electronic packaging materials and technology including TSV and 3D packaging, modeling and simulation, reliability and material characterization, wire bonding and novel solder materials and process etc. He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 20 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

**Companies cited in the report:**


**About Yole Développement**

Founded in 1998, Yole Développement has grown to become a group of companies providing marketing, technology and strategy consulting, media and corporate finance services. With a strong focus on emerging applications using silicon and/or micro manufacturing, the Yole Développement group has expanded to include
more than 50 collaborators worldwide covering MEMS, Compound Semiconductors, LED, Image Sensors, Optoelectronics, Microfluidics & Medical, Photovoltaics, Advanced Packaging, Manufacturing, Nanomaterials and Power Electronics. The group supports industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

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